a planar lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads, wherein the plastic encapsulation is part of a molded cap that covers an array of the device areas.

13. (Amended) An integrated circuit package for accommodating a semiconductor die, comprising:

a planar lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and